CLAIMS

We claim:

1. A method for making a semiconductor device, comprising:

providing a metal structure on a substrate;

providing an insulating layer over the metal structure;

providing a capping structure over the insulating layer; and

annealing the resulting structure.

2. The method of claim 1, wherein the substrate comprises a dielectric upper surface.

3. The method of claim 1, the capping structure comprising a substantially continuous layer.

4. The method of claim 1, the capping structure comprising a dielectric material.

5. The method of claim 4, wherein the dielectric material of the capping structure is PSG.

6. The method of claim 1, wherein the capping structure and annealing decreases peeling of the metal structure when heated.

7. The method of claim 1, including planarizing the insulating layer before providing the capping structure.

8. The method of claim 1, including annealing for about 30 to about 60 minutes at a temperature ranging from about 675 to about 700 degrees Celsius.

9. The method of claim 1, wherein the metal structure comprises tungsten.

14. A method for preventing peeling of a metal structure in a semiconductor device, comprising:

providing a metal structure on a substrate;

providing an insulating layer over the metal structure;

providing a capping structure over the insulating layer; and

annealing the resulting structure.

15. The method of claim 14, wherein a portion of the metal structure has a dimension greater than about 1 micron.

16. A method for preventing peeling of a metal structure in a semiconductor device, comprising:

providing a metal structure on a substrate, the metal structure comprising tungsten and a portion of the metal structure having a dimension greater than about 1 micron; and

providing an insulating layer over the metal structure;

providing a capping structure over the insulating layer; and

annealing the resulting structure;

wherein the annealing decreases peeling of the metal structure when heated.

17. The method of claim 16, wherein a portion of the metal structure has a dimension greater than about 1 micron.

18. A semiconductor device made by the method comprising:

providing a metal structure on a substrate;

providing an insulating layer over the metal structure;

providing a capping structure over the insulating layer; and

annealing the resulting structure.

19. A semiconductor device made by the method comprising:

providing a metal structure on a substrate, the metal structure comprising tungsten and a portion of the metal structure having a dimension greater than about 1 micron; and

providing an insulating layer over the metal structure;

providing a capping structure over the insulating layer; and

annealing the resulting structure;

wherein the capping structure and annealing decreases peeling of the metal structure when heated.

20. A semiconductor device, comprising:

a metal structure on a substrate; a portion of the metal structure having a dimension greater than about 1 micron;

an insulating layer over the metal structure; and

a capping structure over the insulating layer.

21. The device of claim 20, wherein the substrate comprises a dielectric upper surface.

22. The device of claim 20, wherein the capping structure comprises a substantially continuous layer.

23. The device of claim 20, the capping structure comprising a dielectric material.

24. The device of claim 23, wherein the dielectric material of the capping structure is PSG.

25. The device of claim 24, wherein the metal structure comprises tungsten.

26. The device of claim 20, wherein a portion of the metal structure has a dimension smaller than about 0.25 micron.

27. The device of claim 20, wherein the capping structure has been annealed.

28. A semiconductor device, comprising

a metal structure on a substrate; a portion of the metal structure having a dimension greater than about 1 micron and another portion having a dimension less than about 0.25 micron;

an insulating layer over the metal structure; and

a substantially-continuous capping structure over the insulating layer.

29. The device of claim 28, wherein the capping structure has been annealed.

30. A memory device containing an integrated circuit comprising:

a metal structure on a substrate; a portion of the metal structure having a dimension greater than about 1 micron;

an insulating layer over the metal structure; and

a capping structure over the insulating layer.

31. The device of claim 30, wherein the capping structure has been annealed.

32. A memory device containing an integrated circuit comprising:

a metal structure on a substrate; a portion of the metal structure having a dimension greater than about 1 micron and another portion having a dimension less than about 0.25 micron;

an insulating layer over the metal structure; and

a substantially-continuous capping structure over the insulating layer.

33. The device of claim 32, wherein the capping structure has been annealed.

34. An electronic device containing an integrated circuit comprising:

a metal structure on a substrate; a portion of the metal structure having a dimension greater than about 1 micron;

an insulating layer over the metal structure; and

a capping structure over the insulating layer.

35. The device of claim 34, wherein the capping structure has been annealed.

36. An electronic device containing an integrated circuit comprising:

a metal structure on a substrate; a portion of the metal structure having a dimension greater than about 1 micron and another portion having a dimension less than about 0.25 micron;

an insulating layer over the metal structure; and

a substantially-continuous capping structure over the insulating layer.

37. The device of claim 36, wherein the capping structure has been annealed.